Fig 15.49—The synchronous detector operates in the 450- to 455-kHz region. Except as otherwise specified, its fixed-value resistors are 1/4-W, 5%-tolerance units, and its capacitors' working voltages can be 10 or higher. See the References chapter for a list of part suppliers addresses that includes addresses of the firms mentioned below.

D1, D2—BB809 or BB409 tuning diode. Each of these, a "28-V" diode, exhibits approximately 33 pF at 2 V and an unusually high voltage-versus-capacitance slope of 10. Two paralleled 30-V Motorola tuning diodes (one MV2109 [≈45 pF at 2 V] and one MV2105 [≈18 pF at 2 V], both with a slope of 3) may serve as a substitute for each BB809 or BB409.

L1—Approximately 215 μH. Toko RWRS-T1019Z (nominally 220 μH, Q of 100 at 796 kHz, available as Digi-Key Corp no. TK1223), suitable.

R1—50-kΩ trimmer.

R2—10-kΩ linear control.

T1—13 trifilar turns of #28 enameled wire, twisted, on an FT-37-77 toroidal ferrite core.

U1, U2—Signetics NE602N, NE602AN, SA602N, SA602AN mixer/oscillator IC.

U3—Signetics NE604N, NE604AN, SA604N or SA604AN FM receiver subsystem IC.

A Synchronous AM Detector for 455 kHz

Much like switching a receiver or transceiver to SSB and receiving AM as SSB, its carrier at zero beat, synchronous detection overcomes fading-related distortion by supplying an unfading carrier at the receiver. The difference between synchronous AM detection and normal SSB product detection is that synchronous detection *phase locks* its carrier to that of the incoming signal. No tuning error occurs if the received signal happens to fall between a synthesized receiver's tuning steps, and the detector's PLL compensates for modest tuning drift. The result is a dramatic fidelity improvement over diode-detected AM. This circuit, designed by Jukka Vermasvuori, OH2GF, and originally published in July 1993 *QST*, requires only a digital voltmeter for alignment.

The Synchronous Detector Circuit

See **Fig 15.49**. The unit uses popular NE602AN (mixer/oscillator) and NE604AN (FM subsystem) ICs to provide both synchronous and quasi-synchronous detection. (This discussion refers to U1 and U2 as NE602ANs, but NE602Ns, SA602Ns and SA602ANs will work equally well in this application. Likewise, an NE604N, NE604AN, SA604N or SA604AN will work well at U3 in this application.) Operating at a supply voltage of 6, the circuit draws 10 mA. U1, an NE602AN, acts as the BFO and product detector necessary for synchronous detection. Feeding U1's balanced inputs in push-pull helps keep BFO energy from backing out of the input pins and into U3's limiting circuitry. To take advantage of the chip's internal biasing, the input transformer (T1) is isolated with dc blocking capacitors. (U1 also supplies balanced audio output, but usefully reducing this to a single-ended output would have required an operational amplifier. Doing so would reduce even-harmonic distortion in recovered audio, but would not justify the increased circuit complexity and power consumption.)

U1's oscillator amplitude is optimized to 660 mV P-P (as measured across L1) by the 220-Ω resistor at the oscillator output at pin 7. The BFO frequency is adjusted by two variable-capacitance diodes (D1 and D2) in addition to the tank coil, L1. D2 receives its control voltage via switch S3 (BFO MODE), which selects control voltage from either U3's phase detector (SYNC) or a constant voltage from a resistive divider (CW/SSB/TUNE).

The fixed CW/SSB/TUNE voltage (2.16, set by the ratio of R5 and R6) corresponds to the phase detector's optimum output voltage at lock.

R2, BFO TUNING, drives D1 to provide manual detector tuning without upsetting the D2's control-voltage optimization. S2, BFO OFFSET, presets R2's tuning range into the optimum regions for LSB (–2 kHz), DSB AM (±0 kHz) and USB (+2 kHz). (These offsets are for a radio in which received sidebands are inverted relative to their on-air sense.) The BFO TUNING control therefore provides fine adjustment for detector lock around coarse receiver tuning steps (1 kHz in the Sangean AT-808 with which this circuit was originally used).

U3's phase detector requires a 90° phase shift between the incoming and reference phases to give the correct zero-phase output (again, approximately 2.16 V). The all-pass stage, Q1, operates as an isolation stage and adjustable phase shifter to generate the 90° phase shift.

U3 is an NE604N FM IF subsystem IC that contains limiting-amplifier stages (total gain, 101 dB) and a quadrature detector. Band limiting can be inserted between the limiter stages, but experiments with various RC and LC filters brought no improvement, and instead led to increased delay that upset the carrier/sideband phase relationships necessary for good quasi-synchronous detection. The Fig 15.49 circuit uses U3's quadrature detector as a phase detector that outputs control voltage for D2.

The most difficult aspect of the phase-locking chain is the selection of a time constant for the locking loop. Signal fading, in conjunction the relative absence

Quasi-Synchronous Detection

Synchronous detection can be mimicked by amplifying and limiting the AM signal sufficiently (at IF) so that only carrier remains, and substituting this signal for the BFO at the product detector. This *quasi-synchronous detection* acts much like envelope ("diode") detection and works best when the received signal does not fall to zero, as can often occur with SSB and, with AM, during fading. As the signal fades and the carrier-to-noise (C/N) ratio decreases, noise renders the detector's switching action inconsistent, and detection quality deteriorates rapidly. Thus, under conditions of low C/N ratio, quasi-synchronous detection exhibits a distinct detection threshold, as does a diode detector. The chief advantage of quasi-synchronous detection over simple diode rectification is its much lower threshold compared to a diode. The detector circuit presented in Fig 15.49 includes a quasi-synchronous detector for flexibility and A/B comparison with the synchronous circuit.

—Jukka Vermasvuori, OH2GF

or presence of phase-modulation components in the transmitted signal, play important roles in detector lock. Were fading not a problem, a short time constant—one allowing fast locking—would suffice for DSB AM. For SSB AM with carrier (which includes a PM component at all modulation frequencies), however, and DSB AM with fading (during which a fast PLL may unlock on the sudden phase shifts that can accompany fast, deep carrier fades), a long time constant is necessary. Particularly for SSB with carrier, the loop bandwidth must be reduced to below the lowest expected modulation frequency. C1 and R4 set the PLL time constant in Fig 15.49.

The received signal strength indicator (RSSI) output at pin 5 of U3 follows the input level logarithmically, giving an output of 1.1 V on noise only (RF INPUT shorted in Fig 15.49) and 3.3 V at an RF INPUT level of 3 mV. The RSSI output is adaptable as an AGC-detector output, making the NE604AN attractive for simple IF-AGC designs. Because of the NE604AN's high gain, circuit layout can be critical and requires short leads and physically small bypass capacitors. Coupling must be minimized between pin 9 of U3 and the U1 oscillator components.

U2, an NE602AN, operates as a quasi-synchronous detector. The BFO energy it requires is readily available as a square wave at pin 9 of U3. Except for the fact that its BFO input is derived from limited input signal instead of a VCO, U2 functions the same way as U1.

Construction

Two evaluation models were constructed using ground-plane construction, mounting the ICs upside down and soldering their ground pins directly to ground with minimal lead length. The later version is constructed onto a long and narrow piece of circuit board intended to be the bottom plate of an add-on box to be fixed underside of a Sangean ATS-808 receiver. (**Fig 15.50** shows this version's general layout.)

With the circuitry arranged per Fig 15.50 and receiver-detector IF-AF connections made with small-diameter coaxial cable to avoid crosstalk, BFO-signal leakage is unmeasurable at U3; that is, the voltage at RSSI does not change when the BFO is temporarily disabled under no-signal conditions.

Obtaining IF Drive

A simple BJT emitter follower (**Fig 15.51**) can connect the synchronous detector to a solid-state transceiver. The detector can also be driven from the unbypassed cathode resistor of a vacuum-tube receiver's final IF stage (Fig 15.51B). If test equipment is not available to allow accurate measurement of the detector's input level, just keep the detector drive comfortably below that at which distortion begins.

IF signal can be obtained from the ATS-808 receiver via a 56-pF capacitor connected to the hot end of the '808's transformer T9 (at pin 16 of the '808's U1, a TA7758P IC). Connecting the detector cable detunes T9, which, though difficult to reach, must be retuned by turning its slug outwards a few turns to obtain maximum audio output. The detector's audio output (AF OUT) returns to the AT-808 by means of the '808's TONE switch, which

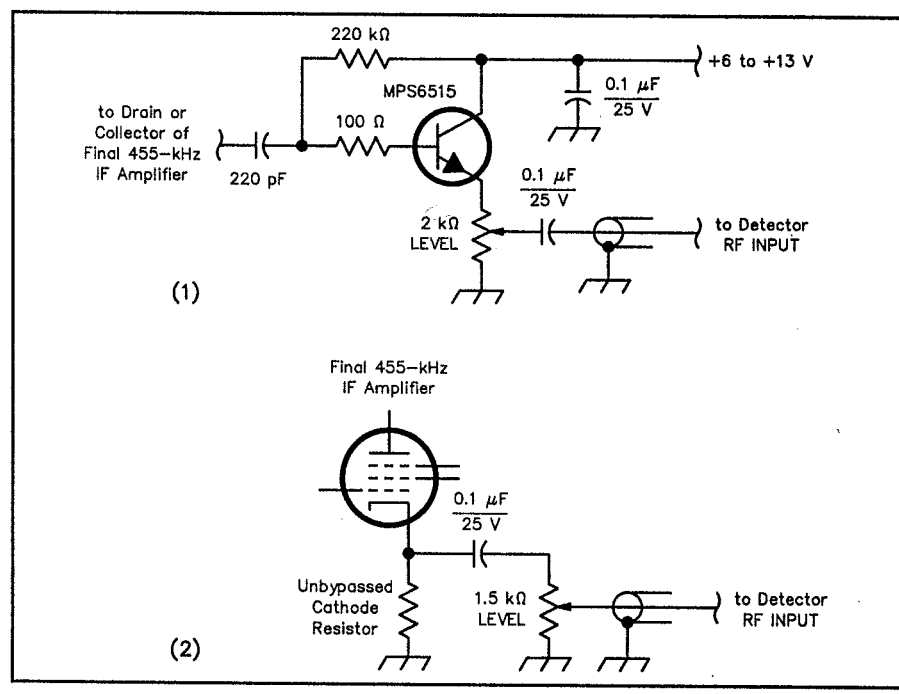

Fig 15.51—Simple circuitry can connect the synchronous detector to a solid-state transceiver (1) or a vacuum-tube receiver (2) if a 455-kHz output tap is not already available.

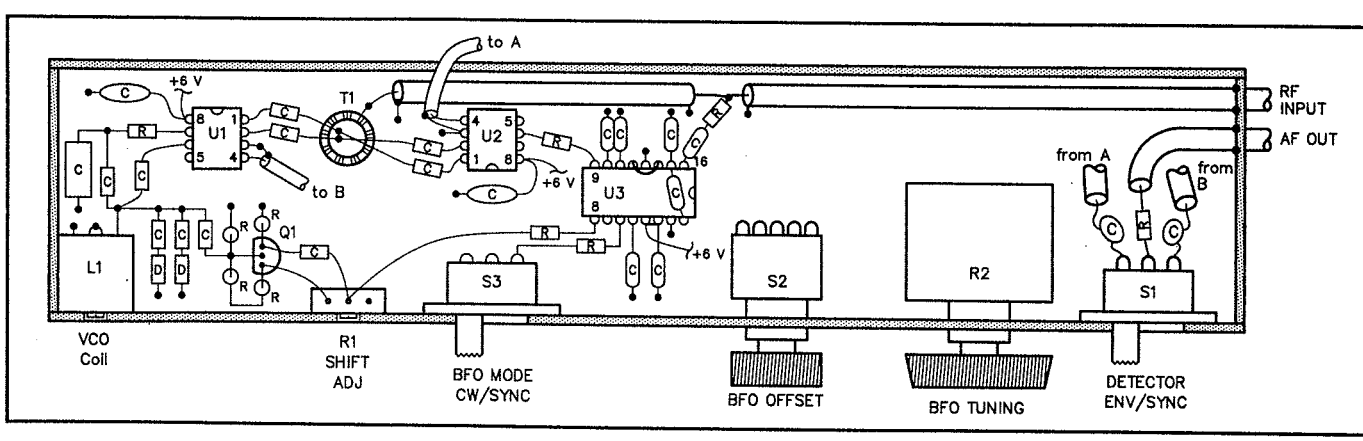

Fig 15.50—One recommended layout for the synchronous detector. U3's high gain requires care in construction—see text.

can be rewired to select audio from the outboard detector.

The key to success with this circuit is getting *interference-free* IF drive. U3's RSSI output can be of critical importance in scoping out possible BFO leakage and/or unwanted signal input. With the detector's RF input shorted, a voltmeter connected to RSSI should indicate about 1.1. If it doesn't, U1's BFO signal may be getting into U3. The RSSI indication shouldn't be much higher than this with the detector connected to the receiver, with the receiver's RF gain control turned all the way down for minimal noise input to the detector. (The receiver used must be in "AM" mode—BFO *off*.) If the RSSI voltage is above the 1-V range at this point, a receiver oscillator or some other signal, however inaudible, may be driving U3's limiter. *The detector will be unable to achieve and hold lock if anything other than the receiver IF signal captures its limiter.* The NE604's limiter stages, specified to work up to at least 21 MHz, are capable of 101 dB of overall gain and specified to be several decibels into limiting with *as little as 3 mV* (–92 dBm) applied across a 50-Ω load at the '604's input!

Operation

After checking the circuit, connect it to a 6-V power supply. The total current consumption should be approximately 10 mA. Switch the DETECTOR switch to ENVELOPE; band noise should now be audible. Tune in a strong AM signal, switch S3, BFO MODE, to SSB/CW/TUNE, and set the DETECTOR switch to SYNC. The detector may sound very quiet at this point. Adjust L1's core until the signal swoops into audibility. This proves that the BFO is oscillating. If possible, measure the BFO level across L1 with an oscilloscope and 10:1 probe; it should be about 660 mV. (If test-equipment unavailability disallows this measurement, go to the next paragraph.) If it's not, experiment with R3's value to make it so.

Accurately tune the receiver to a strong, pure carrier, such as a beacon. Adjust R2, BFO TUNING, for a wiper voltage of 2.00 with S2, BFO OFFSET, set to ±0 kHz. Mark as CENTER this point in its knob's travel. With the BFO MODE, switch in the SSB/CW/TUNING position, use a nonmetallic tool to adjust L1, the VCO coil, for zero beat with the incoming carrier. Returning S3 to the SYNC position should allow carrier lock if R1, SHIFT ADJ, is reasonably near adjustment. Adjust SHIFT ADJ for carrier lock if necessary. This completes coarse adjustment of SHIFT ADJ. Return the BFO MODE switch to the SSB/CW/TUNING position; the BFO should still be at or very close to zero beat with the incoming signal.

Return the BFO MODE switch to the SYNC position. After the detector locks, fine-tune SHIFT ADJ to minimize detected low-frequency hiss. (If a sufficiently strong unmodulated local signal is not available off-air, transmit into a dummy antenna with a PLL-synthesized transceiver and make this adjustment by listening to its signal. It should be possible to find a SHIFT ADJ setting at which detected hiss distinctly nulls. As a less desirable alternative, tune in an unfading AM signal modulated with a 1-kHz tone and adjust SHIFT ADJ for maximum tone recovery.) Once this is done, the detector's carrier phase is within exactly 0° or 180° of the BFO signal applied to the amplitude detector (U1), and the detector's response to phase noise has been minimized. Also significantly, this alignment procedure sets the detector to lock in a range centered on the control voltage that corresponds to optimum locking sensitivity *and* minimum phase noise demodulation. This completes alignment.

To zero-beat and lock a given station: Set the BFO TUNING control to its center (2.00 V) position, BFO MODE switch to CW/SSB/TUNE and BFO OFFSET to match the sideband(s)—LSB, USB or both—desired. Tune the receiver as close to zero beat as its tuning steps allow. Adjust BFO TUNING for zero beat. Switch the BFO MODE switch to SYNC to lock the detector.

Toggling S1, DETECTOR, between ENVELOPE and SYNC allows easy comparison of the effects of detection mode under adverse propagation conditions. The synchronous mode will be considerably superior much of the time. The quasi-synchronous (ENVELOPE) mode may give crisper audio under average or poor signal conditions; this effect may be due to increasing distortion as the signal approaches the noise floor, however.

Properly adjusted, the synchronous detector operates at less than 1% total harmonic distortion. (The quasi-synchronous detector provides comparable performance—but only on a nonfading test signal.) Measurements confirm the importance of setting R1, SHIFT ADJ, properly: Improper adjustment can increase low-order harmonic-distortion products by 3 to 12 dB in addition to increasing the detector's sensitivity to phase noise.

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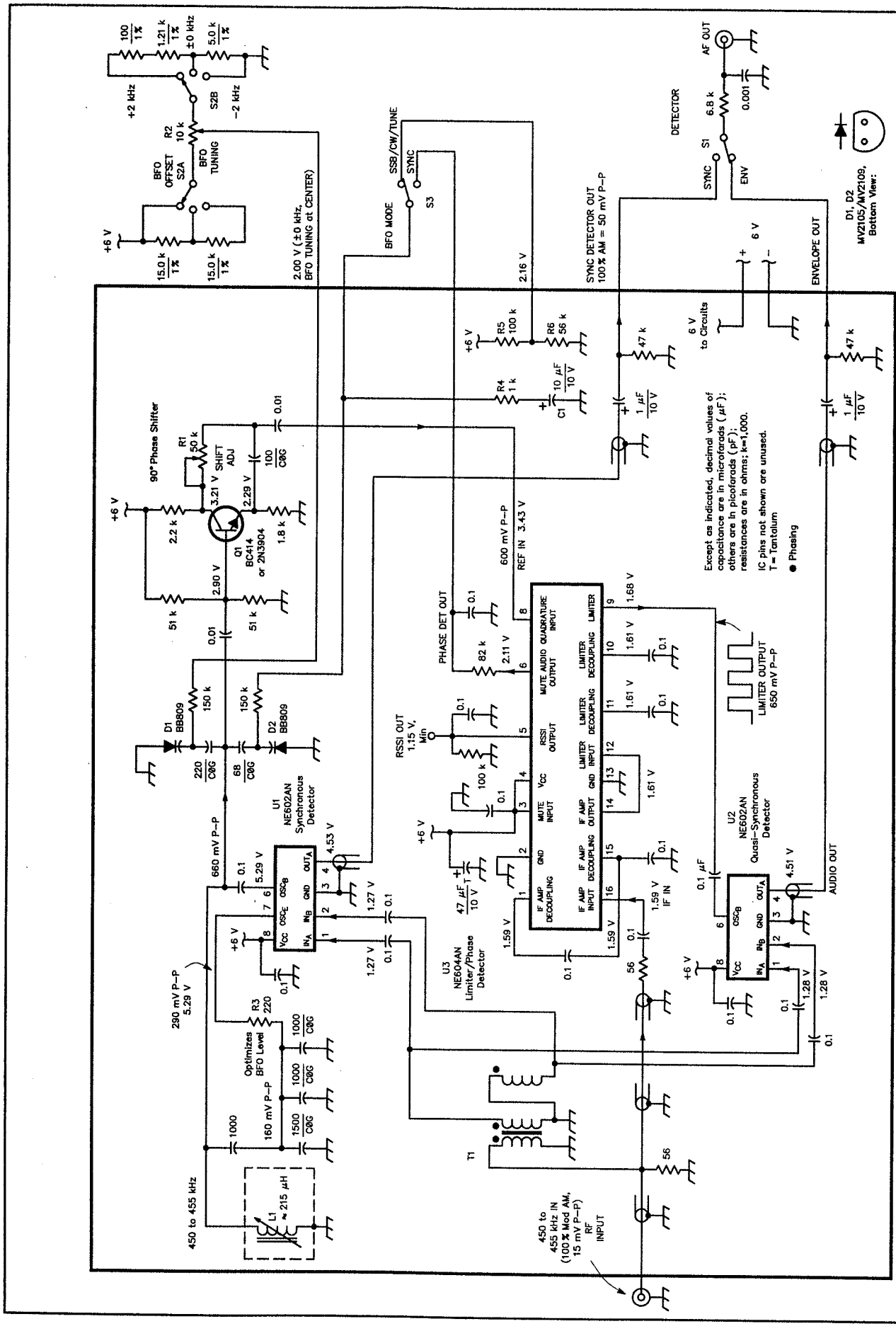
90° Phase Shifter
SHIFT ADJ
Q1 BC414 or 2N3904
U1 NE602AN Synchronous Detector
U2 NE602AN Quasi-Synchronous Detector
U3 NE604AN Limiter/Phase Detector
BFO OFFSET S2A
BFO TUNING
S2B
BFO MODE
SSB/CW/TUNE
SYNC
S3
DETECTOR
SYNC
ENV
S1
AF OUT
SYNC DETECTOR OUT 100% AM = 50 mV P-P
ENVELOPE OUT
6 V to Circuits
REF IN 3.43 V
PHASE DET OUT
RSSI OUT 1.15 V, Min
LIMITER OUTPUT 650 mV P-P
AUDIO OUT
IF IN
450 to 455 kHz
450 to 455 kHz IN (100% Mod AM, 15 mV P-P) RF INPUT
Optimizes BFO Level
D1, D2 MV2105/MV2109, Bottom View:
Except as indicated, decimal values of capacitance are in microfarads (μF); others are in picofarads (pF); resistances are in ohms; k=1,000.
IC pins not shown are unused.
T = Tantalum
● Phasing